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	L #	Hits	Search Text	DBs	Time Stamp
1	L2	49	("6107141") or ("6133098") or ("6187636") or ("6228695") or ("6294297") or ("6436764") or ("6566196") or ("6635533") or ("6660589") or ("6764905") or ("6803276") or		2005/07/01 09:02
2	L4	17	1" 74 4 5 5 4 "   " 7 7 8 7 5 5 7 "	3	2005/07/01 09:22
3	L5	16	("6040216").URPN.	ILICIDATI	2005/07/01 09:41
4	L6	107745	"nonvolatile memory" or "flash memory"		2005/07/01 09:48

	L #	Hits	Search Text	DBs	Time Stamp
5	L7 ·	6483	(select near gate)	US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B	2005/07/01 09:48
6	L8	62524	(control near gate)		2005/07/01 09:48
7	L9	31793	(floating near gate)	US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B	2005/07/01 09:49
8	L10	1214	7 same 8 same 9	US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B	2005/07/01 09:49

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9	L11	862	10 and 6	US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B	2005/07/01 09:49
10	L12	779	11 and ((@ad<"20030730") or (@rlad<"20030730"))		2005/07/01 09:51
11	L13	524	12 and (poly-si or polysilicon)	US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B	2005/07/01 09:58
12	L14	505	13 and (memory adj cell)	US- PGPUB; USPAT; EPO; JPO; DERWEN T; IBM_TD B	2005/07/01 09:58
13	L15	4 ·	("5874759"   "6091104"   "6291297"   "6476440").PN.		2005/07/01 10:24

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14	L16	3	("6747310").URPN.	USPAT	2005/07/01 10:25
15	L17	3	("6747310").URPN.	USPAT	2005/07/01 10:25

US-PAT-NO:

6747310

DOCUMENT-IDENTIFIER:

US 6747310 B2

TITLE:

Flash memory cells with separated self-aligned

select

and erase gates, and process of fabrication

----- KWIC -----

Abstract Text - ABTX (1):

**Flash memory** and process of fabrication in which vertically stacked pairs of

<u>floating gates and control gates</u> are formed on opposite sides of a source

diffusion in a substrate, an erase gate is formed directly above the source

diffusion and between the stacked  $\underline{\text{gates}}$ ,  $\underline{\text{select gates}}$  are formed on the sides

of the stacked gates opposite the erase gate, programming paths extend from

mid-channel regions in the substrate between the  $\frac{\text{select gates}}{\text{stacked}}$  and the

gates to the edge portions of the **floating gates** which face the **select gates**,

and erase paths extend from the edge portions of the  $\frac{\text{floating gates}}{\text{hich face}}$ 

the erase gates to the source diffusion and to the erase gate. In some

embodiments, the source regions are connected electrically to the erase gates,

and in others the  $\underline{\textbf{floating gates}}$  project laterally beyond the  $\underline{\textbf{control}}$  gates on

one or both sides of the  $\underline{\text{control gates}}$ . These  $\underline{\text{memory cells}}$  are very small in

size and provide substantially better programming and erase performance than

memory cells of the prior art.

Application Filing Date - AD (1): 20021007

TITLE - TI (1):

Flash memory cells with separated self-aligned select and erase
gates, and
process of fabrication

Brief Summary Text - BSTX (3):

particularly, to nonvolatile memory and the manufacture thereof.

Brief Summary Text - BSTX (5):

<u>Nonvolatile memory</u> is currently available in several forms, including

electrically programmable read only memory (EPROM), electrically erasable

programmable read only memory (EEPROM), and flash EEPROM.

Brief Summary Text - BSTX (6):

U.S. Pat. Nos. 6,091,104 and 6,291,297 show a split-gate **memory** cell of

relatively small size, efficient erase performance, and relatively programming

current requirements. The small size is obtained through self-alignment of the

select, control and floating gates, and the efficiency in erasing is provided

by the use of Fowler-Nordheim tunneling from a sharply rounded side edge of the

floating gate to the select gate. The programming current is kept small by the

use of mid-channel hot carrier injection from the off-gate channel region

between the select gate and the floating gate to the sharply curved side edge

of the floating gate.

Brief Summary Text - BSTX (7):

A <u>memory cell</u> of this type is illustrated in FIG. 1 as having a floating

gate 16, a control gate 17, and select gate 18, all of which are
fabricated of

polysilicon. The control gate is stacked above the floating gate, and the

select gate is positioned to the side of the stacked gates. With the
three

polysilicon
fabrication process,

this type of cell is sometimes referred to as a 3P self-aligned split gate cell.

Brief Summary Text - BSTX (8):

In the programming mode, the  $\underline{\text{control gate}}$  is biased at a voltage of about 10

volts, the <u>select gate</u> is biased at about -2 volts, and the source 19 is biased

at about -6 volts. The strong electric field thus established across the

mid-channel gate oxide 21 between **select gate** 18 and **floating gate** 16 causes.

electrons to be accelerated and injected into the  $\underline{\textbf{floating gate}}$ , as indicated by arrow 22.

Brief Summary Text - BSTX (9):

In the erase mode, a negative voltage of about -10 volts is applied to the

control gate, and a positive voltage of about 6 volts is applied to the select

gate. In this mode, the electric field across the inter-poly oxide
23 between

the <u>select gate</u> and the rounded side wall 24 of the <u>floating gate</u> initiates

Fowler-Nordheim tunneling, with electrons flowing from the <a href="floating">floating</a> gate to the

select gate, as indicated by arrow

Brief Summary Text - BSTX (10):

While the 3P self-aligned split gate cell structure and the unique programming and erase techniques employed with it permit a smaller cell size

than the widely used ETOX structure, as cell sizes decrease into the range of

hundreds of nanometers, it is limited by the need to remove polysilicon from

the source region and in the narrow, steep valleys between adjacent control and  $\dot{\phantom{a}}$ 

floating gate stacks.

Brief Summary Text - BSTX (12):

It is in general an object of the invention to provide a new and improved

flash memory cell and fabrication process.

Brief Summary Text - BSTX (13):

Another object of the invention is to provide a **memory cell** and process of

the above character which overcome the limitations and disadvantages of the prior art.

Brief Summary Text - BSTX (14):

Another object of the invention is to provide a  $\underline{\text{memory cell}}$  and process of

the above character in which the  $\underline{\text{memory cell}}$  is very small in size and provides

significantly enhanced programming and erase performance.

Brief Summary Text - BSTX (15):

These and other objects are achieved in accordance with the invention by

providing a <u>flash memory</u> and process of fabrication in which vertically stacked

pairs of **floating gates and control gates** are formed on opposite sides of a

source diffusion in a substrate, an erase gate is formed directly above the

source diffusion and between the stacked  $\underline{\mathtt{gates}}$ ,  $\underline{\mathtt{select}}$  are formed on the

sides of the stacked gates opposite the erase gate, programming paths extend

from mid-channel regions in the substrate between the **select gates** and the

stacked gates to the edge portions of the  $\underline{\textbf{floating gates}}$  which face the  $\underline{\textbf{select}}$ 

gates, and erase paths extend from the edge portions of the floating
gates

which face the erase gates to the source diffusion and to the erase gate. In

some embodiments, the source regions are connected electrically to the erase

gates, and in others the **floating gates** project laterally beyond the **control** 

gates on one or both sides of the control gates. These memory cells
are very

small in size and provide substantially better programming and erase performance than **memory cells** of the prior art.

Drawing Description Text - DRTX (2):

FIG. 1 is a cross-sectional view of a split-gate NOR **flash memory** cell

structure of the prior art.

Drawing Description Text - DRTX (3):

FIGS. 2A and 2B are cross-sectional views, somewhat schematic, taken along

line 2--2 in FIG. 5, of two embodiments of a self-aligned split-gate  ${\tt NOR-type}$ 

flash memory cell array according to the invention.

Drawing Description Text - DRTX (4):

FIGS. 3A and 3B are cross-sectional views, similar to FIGS. 2A and 2B, of

another two embodiments of a self-aligned split-gate NOR-type  $\underline{\textbf{flash}}$   $\underline{\textbf{memory cell}}$ 

array according to the invention.

Drawing Description Text - DRTX (5): FIGS. 4A-4E are cross-sectional views

FIGS. 4A-4E are cross-sectional views, similar to FIGS. 2A and 2B, of

additional embodiments of a self-aligned split-gate NOR-type flash
memory cell

array according to the invention.

Drawing Description Text - DRTX (7):

FIGS. 6A-6E are schematic cross-sectional views illustrating the steps in  $% \left( 1\right) =\left( 1\right) +\left( 1\right) +$ 

one embodiment of a process for fabricating a NOR-type **flash memory cell** array

in accordance with the invention.

Drawing Description Text - DRTX (8):

FIGS. 7A-7E are schematic cross-sectional views illustrating the steps in a  $\,$ 

second embodiment of a process for fabricating a NOR-type  $\underline{\textbf{flash}}$   $\underline{\textbf{memory cell}}$ 

array in accordance with the invention.

Drawing Description Text - DRTX (9):

FIGS. 8A-8D are schematic cross-sectional views illustrating the steps in a  $\,$ 

third embodiment of a process for fabricating a NOR-type **flash memory** cell

array in accordance with the invention.

Detailed Description Text - DETX (2):

In the embodiments of FIGS. 2A and 2B, two  $\underline{\text{memory cells}}$  28 share a common

erase gate 29. Each cell has vertically stacked, self-aligned floating and

control gates 31, 32, with the floating gate 31 being relatively thin
(e.g.,

100 .ANG.-700 .ANG.) and the **control gate** 32 positioned above the **floating** 

gate. Each cell also has a select gate 33 which is positioned to one side of

the stacked floating and control gates. The select gates and the erase gate

are formed simultaneously from a layer of  $\underline{\textbf{polysilicon}}$  which is deposited across

the wafer, then etched anisotropically in a dry etching process.

Detailed Description Text - DETX (4):

In these embodiments, programming takes place in the mid-channel regions 37

between the select gates and the floating gates. During a

programming

operation, the <u>control gate</u> is biased to about -10 volts, the <u>select</u> gates are

biased to about 1-3 volts, the source region is biased to about -6 volts, and

the drain region is grounded. These biasing conditions produce a strong,

vertically oriented electric field in the channel regions 37 between the  $\mathbf{select}$ 

gates and the floating gates, with electrons being delivered to the edge

portions of the **floating gates** by hot electron injection from the channel

regions, as indicated by arrows 38. This is sometimes referred to as source-side injection.

Detailed Description Text - DETX (5):

In contrast to the prior art where erasing is done on the same side of the

floating gate as programming, in the **memory cells** of the present invention,

programming and erasing are done on opposite sides of the floating gate. The

shared erase gate and the source diffusion are either independently biased or

electrically connected to facilitate electron tunneling during erase operations.

Detailed Description Text - DETX (9):

The cell structure shown in FIGS. 3A and 3B is similar to that of FIGS. 2A

and 2B, and like reference numerals designate corresponding elements in the

different embodiments. In the embodiments of FIGS. 3A and 3B, however, source

diffusion 34 and erase gate 29 are tied together electrically, and an erase

operation is performed by biasing **control gates** 32 negatively to a level of

about -10 volts, with the source and erase gate node at about 6 volts, and the

select gate and drain floating. This creates a strong, but uniformly
distributed electric field along the edge of floating gate,
surrounded by the

erase gate and the underlying source diffusion, and electrons tunnel from the

floating gate both to the erase gate and to the source region, as
indicated by

arrows 42, 43. Erase efficiency is thus greater than it is with only inter-poly tunneling, and band-to-band tunneling is suppressed by the

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